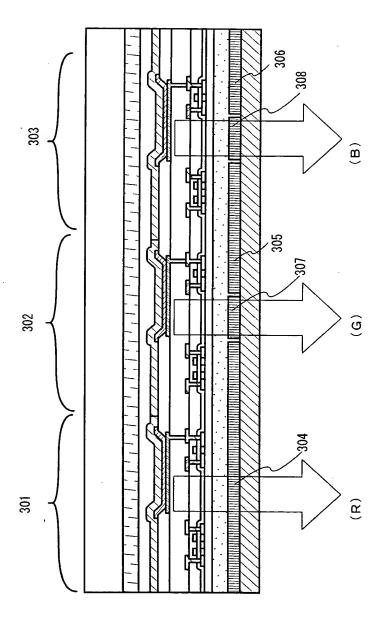


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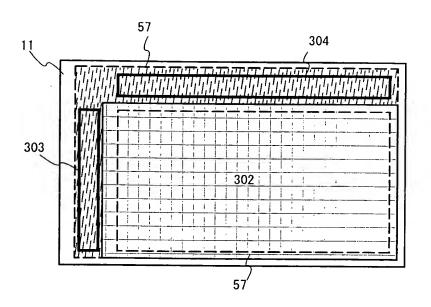
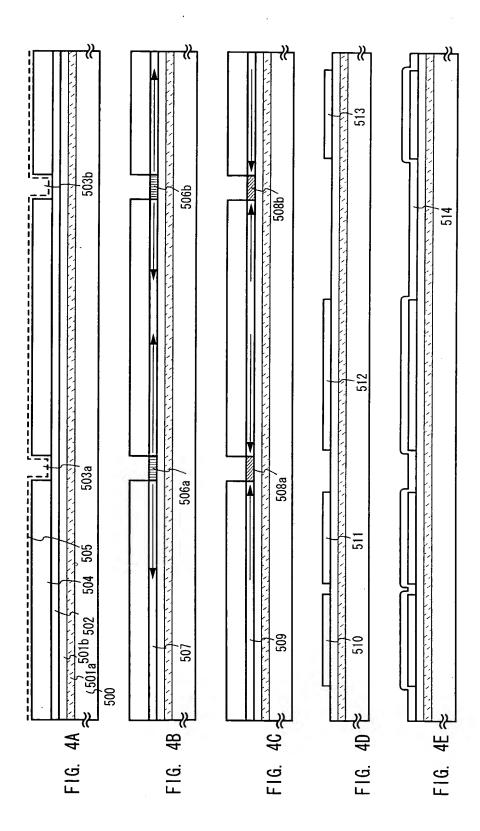
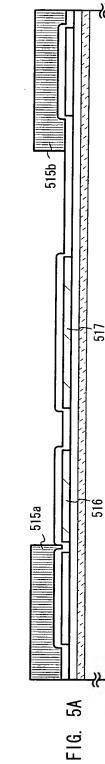


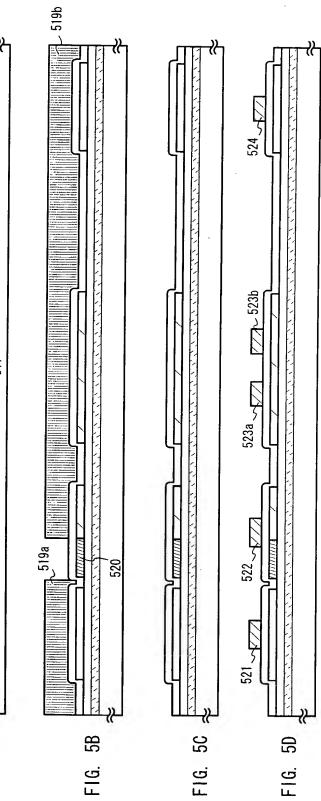
FIG. 3

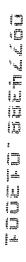


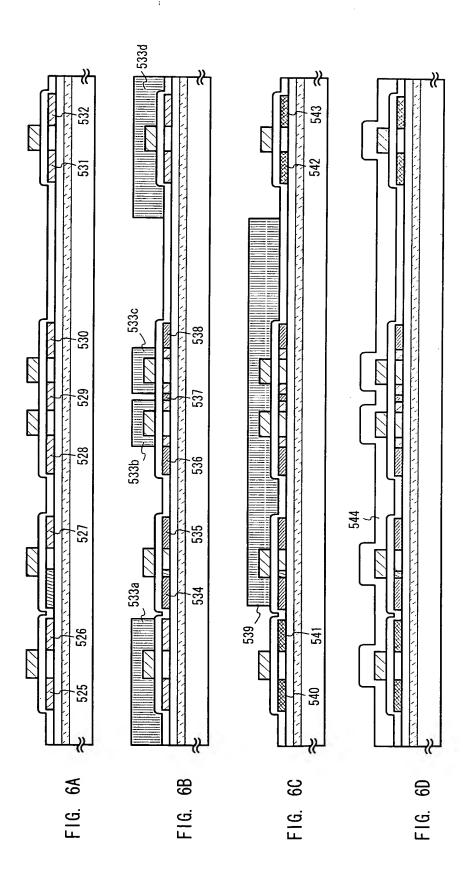


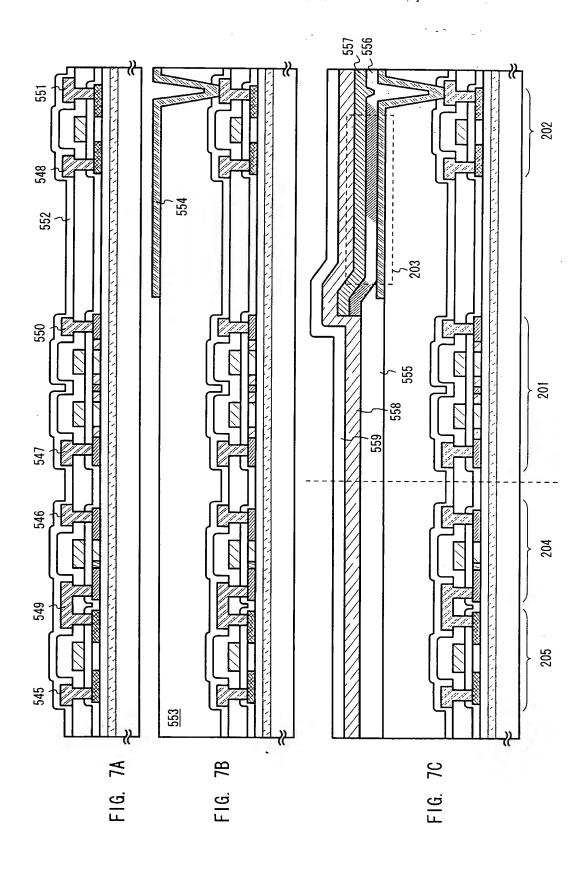
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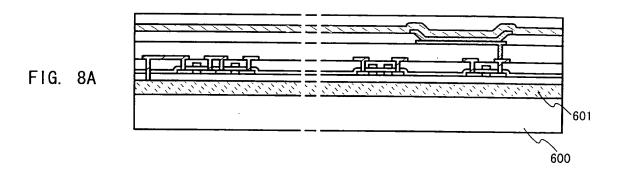


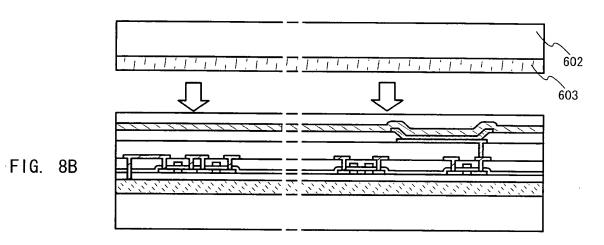


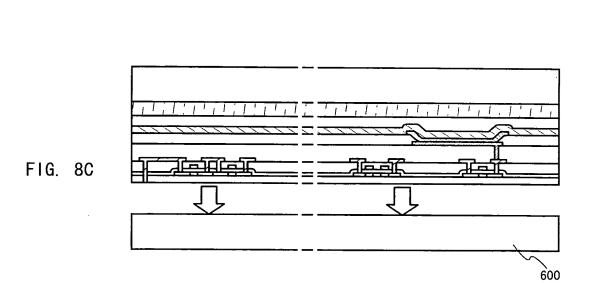












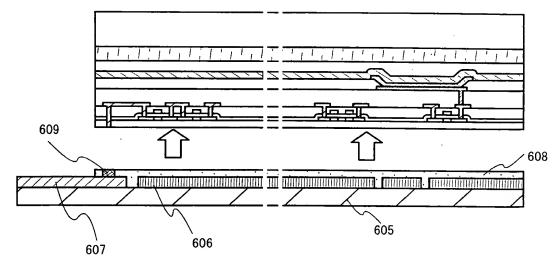


FIG. 9A

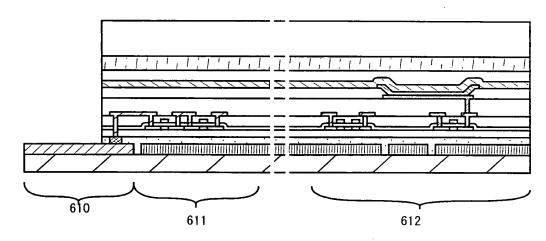


FIG. 9B

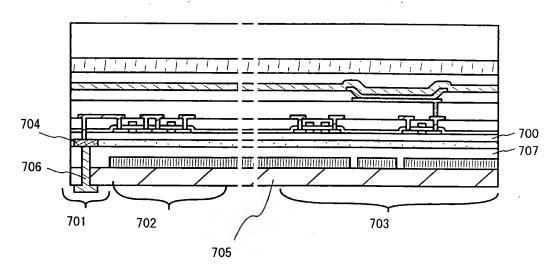


FIG. 10A

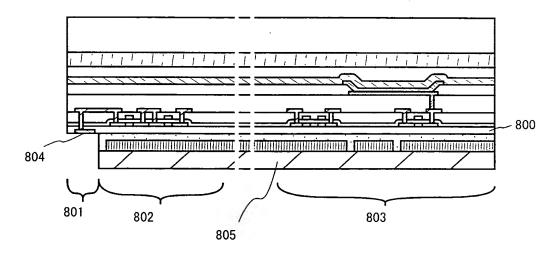


FIG. 10B

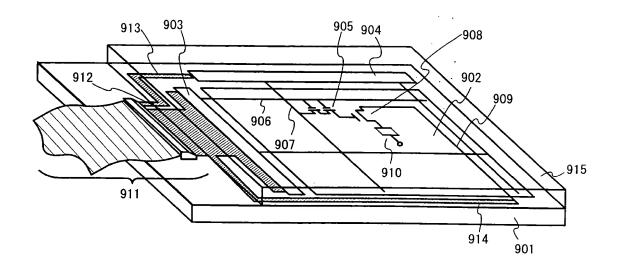
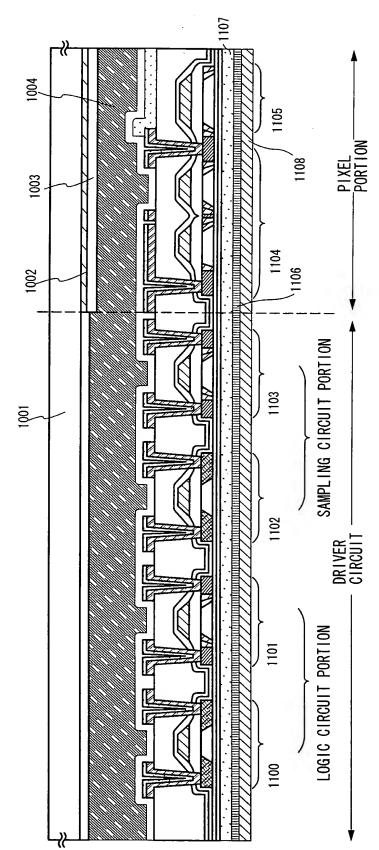


FIG. 11



F1G. 12

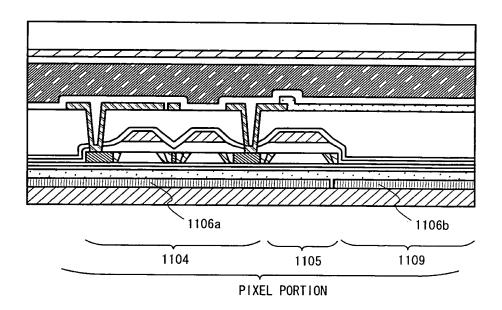


FIG. 13

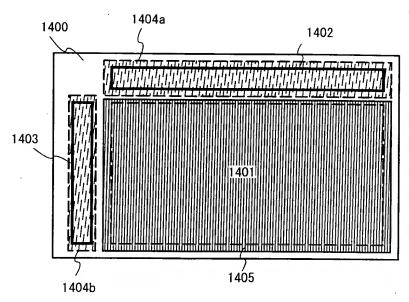


FIG. 14A

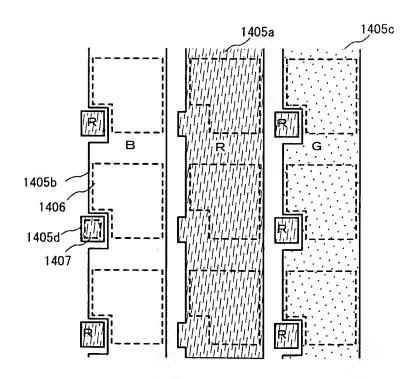


FIG. 14B

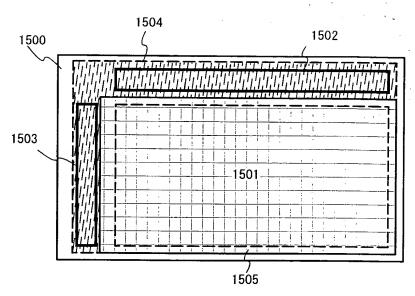


FIG. 15A

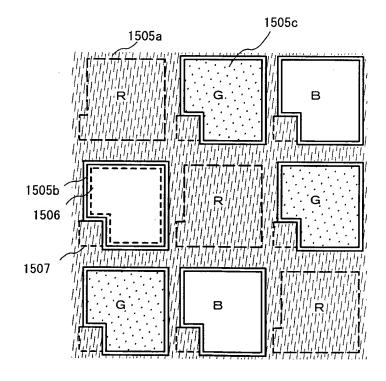
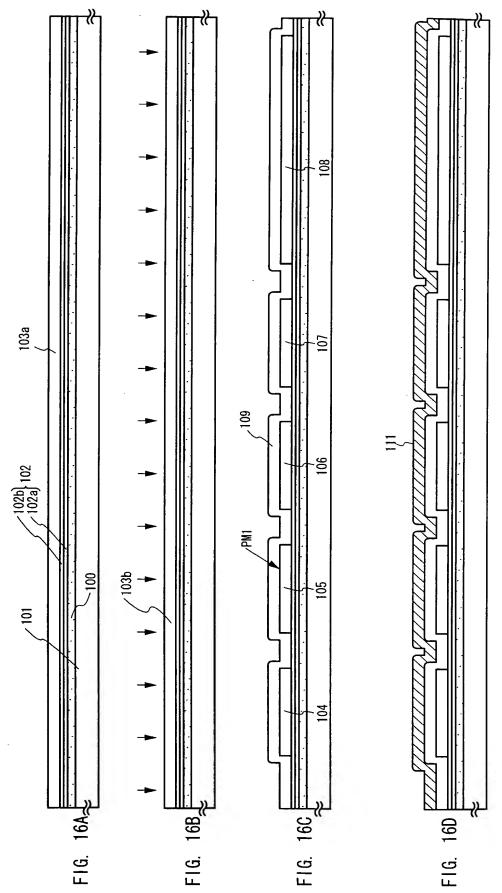
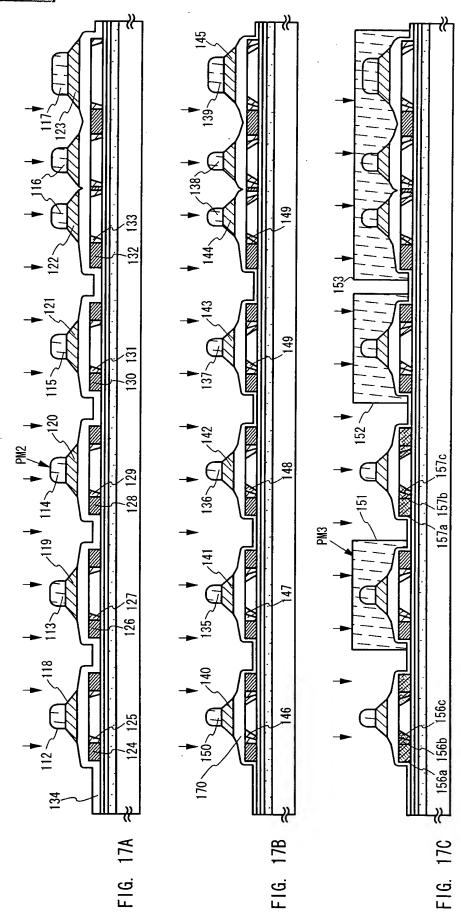
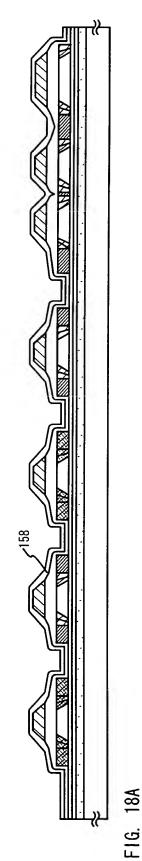


FIG. 15B



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180 1215a 215b 215c 214a 216 214b 217 219a 219b 🍫 1105 169a 169b PIXEL PORTION PM5 1104 164b .164a SAMPLING CIRCUIT PORTION 1103 PM4 PM 159 160a <sub>/</sub>160b 165a <sup>165b</sup> 166a <sup>166b</sup> 161a 161b162a 163b 167a <sup>167b</sup>168a <sup>168b</sup> 1102 208 211a 211b 211c DRIVER CIRCUIT LOGIC CIRCUIT PORTION 1101 207a 207b 207c 206 209a 209b 209c 1100

F1G. 18B

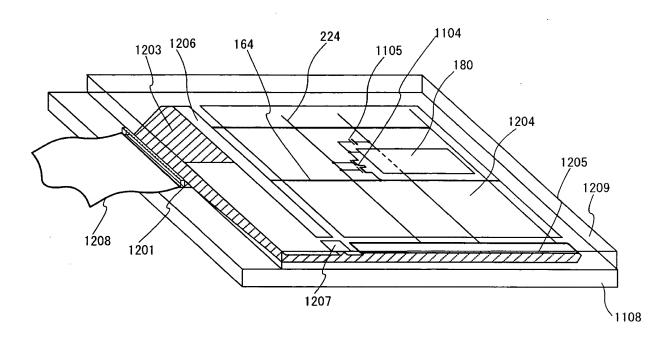


FIG. 19

APPROVED O.G. FIG.

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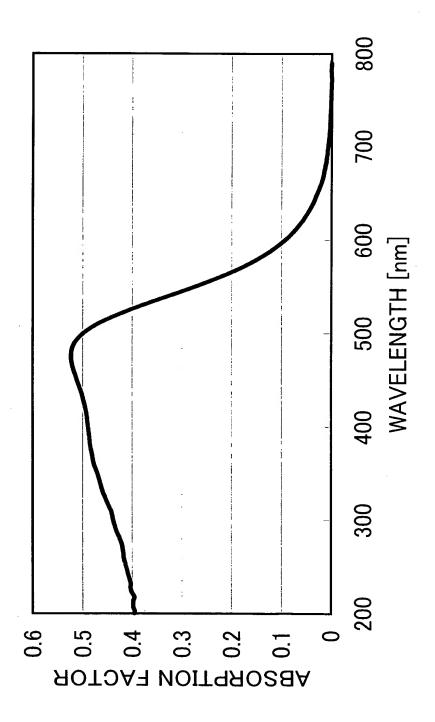


FIG. 20

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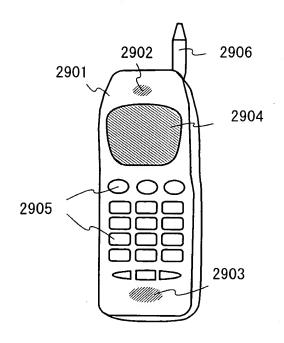


FIG. 22A

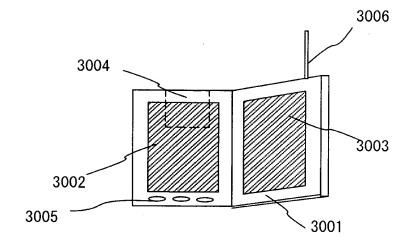


FIG. 22B

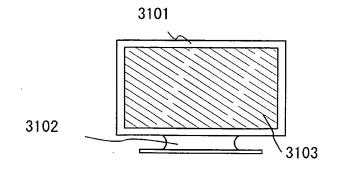


FIG. 22C